

REMARKS

In the present Application, Claims 1-8 and 12-16 are pending. Claims 1-8 and 12-16 are rejected. By this response, claims 1-8 and 12-16 continue without amendment. Claims 9-11 have been cancelled. In view of the following discussion, the Applicant submits that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102. Thus, the Applicant believes that all of these claims are now in condition for allowance.

I. Rejection of Claims under 35 U.S.C. §102

Claims 1-8 and 12-16 are rejected under 35 U.S.C. §102(e) as being anticipated by Chung et al. (U.S. Patent No. 6,680,218 B2) ("Chung"). The Examiner separately rejected claims 1-8 and 12-15 as being anticipated by Chance et al. (U.S. Patent No. 5,177,594) ("Chance"). These rejections are respectfully traversed.

A. Rejection under Chung

The Examiner stated that Chung shows an integrated circuit package 306 having an array of landing pads on the top surface and an array of solder balls 142 disposed on the outside surface. (Office Action, pp. 2-3) (citing Chung, FIG. 5). The Examiner further stated that Chung teaches an interposing structure 304 coupling a first micro-bump on a die to a first landing pad on the integrated circuit package located opposite the first micro-bump and to a second landing pad on the integrated circuit package. (Office Action, p. 2) (citing Chung, FIG. 5). Applicant respectfully disagrees.

Chung describes an IC 302 and an IC package consisting of a vertical package section 304 and a horizontal package section 306. The IC 302 is flip-chip mounted to the vertical section 304 using solder bumps. (Chung, col. 3, line 55 through col. 4, line 18; FIG. 3). Bond pads on the bottom surface of the vertical section 304 are electrically connected to bond pads on the top surface of the horizontal section 306. (Chung, col. 5, lines 45-55; col. 8, lines 5-10). As shown in each of the Figures in Chung, the vertical section 304 couples the solder bumps of the IC 302 to the bond

pads on the horizontal section 306 in a 1-1 fashion, i.e., each solder bump on the IC is coupled to one bond pad located opposite the solder bump.

In view of the forgoing, Chung does not teach or suggest each and every element of Applicant's claim 1. Namely, Chung does not teach or suggest an interposer that couples a first micro-bump on the IC die to both a first landing pad located opposite the first micro-bump and to a second landing pad, each of which being on an inside surface of an integrated circuit package. In contrast, Chung describes and shows that each of the solder bumps on the IC 302 is coupled to a single one of the bond pads on the horizontal section 306. There is no teaching or suggestion in Chung that one of the solder bumps on the IC 302 is coupled to both a bond pad opposite the solder bump and another bond pad on the horizontal section.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."
Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Chung does not teach an interposer that couples a first micro-bump on the IC die to both a first landing pad located opposite the first micro-bump and to a second landing pad, each of which being on an inside surface of an integrated circuit package. As such, Chung does not teach each and every element of Applicant's claim 1 as arranged therein. Accordingly, Chung does not anticipate Applicant's invention recited in claim 1.

Claim 12 includes features similar to those of claim 1 emphasized above. For the same reasons set forth above, the Applicant contends that Chung does not anticipate the invention of claim 12. Claims 2-8 and 14-16 depend, either directly or indirectly, from claims 1 and 12 and recite additional features therefor. Since Chung does not anticipate Applicant's invention as recited in claims 1 and 12, dependent claims 2-8 and 14-16 are also not anticipated and are allowable.

Therefore, the Applicant contends that claims 1-8 and 12-16 are not anticipated by Chung and, as such, fully satisfy the requirements of 35 U.S.C. §102. The Applicant respectfully requests that the present rejection be withdrawn.

B. Rejection under Chance

The Examiner stated that Chance shows an integrated circuit package 54 having an array of landing pads on the top surface and an array of pins disposed on the outside surface. (Office Action, p. 5) (citing Chance, FIG. 1). The Examiner further stated that Chance teaches an interposing structure 50 coupling a first micro-bump on a die to a first landing pad on the integrated circuit package located opposite the first micro-bump and to a second landing pad on the integrated circuit package. (Office Action, p. 5) (citing Chance, FIG. 1). The Examiner stated that the coupling of the first micro-bump to the second landing pad is inherent. Applicant respectfully disagrees.

Chance describes an interposer module 50 supporting an IC 52 and mounted on a ceramic interconnection substrate 54. The IC 52 and the interposer module 50 are joined to their respective surfaces by solder balls 56. (Chance, col. 4, lines 10-22; FIG. 1). Vias 64 in the interposer module 50 couple specific ones of the upper and lower solder balls 56. (Chance, col. 4, lines 40-42; FIG. 1). As shown in FIG. 1, the vias 64 in the interposer module 50 couple the solder balls of the IC 52 to the solder balls on the substrate 54 in a 1-1 fashion, i.e., each solder ball on the IC 52 is coupled to an oppositely located solder ball on the substrate 54.

In view of the forgoing, Chance does not teach or suggest each and every element of Applicant's claim 1. Namely, Chance does not teach or suggest an interposer that couples a first micro-bump on the IC die to both a first landing pad located opposite the first micro-bump and to a second landing pad, each of which being on an inside surface of an integrated circuit package. In contrast, Chance describes and shows that each of the solder balls on the IC 52 is coupled to a single one of the solder balls on the substrate 54. There is no teaching or suggestion in Chance that one of the solder balls on the IC 52 is coupled to both an oppositely located solder ball (or bond pad) and another solder ball (or bond pad) on the substrate.

Furthermore, to establish anticipation by inherency, extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. USA v. Monsanto Co., 948 F.2d 1264, 1268 (Fed. Cir. 1991). The Examiner has not provided any evidence that Chance inherently teaches an interposer that couples a solder ball to both an oppositely located solder ball (or bond pad) and another solder ball (or bond pad) on the substrate. Notably, it is not necessarily the case, since the drawings in Chance show the exact opposite. That is, the drawings show 1-1 connectivity between the solder balls on the IC and the solder balls on the substrate.

Chance does not teach an interposer that couples a first micro-bump on the IC die to both a first landing pad located opposite the first micro-bump and to a second landing pad, each of which being on an inside surface of an integrated circuit package. As such, Chance does not teach each and every element of Applicant's claim 1 as arranged therein. Accordingly, Chance does not anticipate Applicant's invention recited in claim 1.

Claim 12 includes features similar to those of claim 1 emphasized above. For the same reasons set forth above, the Applicant contends that Chance does not anticipate the invention of claim 12. Claims 2-8 and 14-15 depend, either directly or indirectly, from claims 1 and 12 and recite additional features therefor. Since Chance does not anticipate Applicant's invention as recited in claims 1 and 12, dependent claims 2-8 and 14-15 are also not anticipated and are allowable.

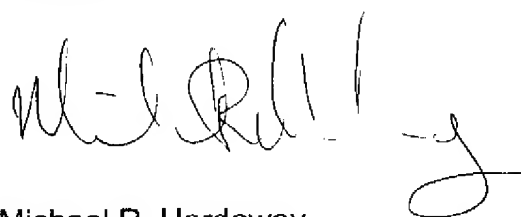
Therefore, the Applicant contends that claims 1-8 and 12-15 are not anticipated by Chance and, as such, fully satisfy the requirements of 35 U.S.C. §102. The Applicant respectfully requests that the present rejection be withdrawn.

II. CONCLUSION

Thus, Applicant submits that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102. Consequently, Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Applicant's Attorney at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,



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I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on December 12, 2007.

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